REMARKS

Claim 26 is objected to due to an informality. Claim 26, which depends from Claim 21, has been cancelled, as the recitations of Claim 26 have been included in amended Claim 21.

In light of the cancellation of Claim 26, applicant respectfully requests withdrawal of the objection to Claim 26.

Claim Rejections Under 35 USC § 102

Claims 1, 2, 5, 6, 10 - 17, 19, 20, 29, 30, and 32 are rejected under 35 USC § 102(b) as being anticipated by U.S. Patent No. 6,146,970, to Witek et al.

Applicant respectfully contends that the Witek et al. reference does not even suggest applicant's invention as described in his specification and as claimed in the claims as amended herein.

Witek et al. pertains to a method for forming a capped shallow trench isolation (CASTI) structure. At Col. 6, lines 14 - 16, the Witek et al. reference describes the formation of a thin layer 204 of thermally-grown silicon oxide having a thickness between roughly 50 Å and 250 Å, with a thickness of roughly 150Å being preferred. At Col. 6, lines 45 - 60, the Witek et al. reference describes the RIE etching of a trench into a silicon substrate, followed by a creation of a thin thermal oxide liner 212 over the surface of the etched silicon trench. At Col. 6, lines 49 - 51, Witek et al. discloses that the height of the trench (depth into the substrate) is typically between about 3,000 Å and 7,000 Å (0.3 μm and 0.7 μm). At Col. 7, lines 5 - 6, the Witek et al. reference teaches that the liner 212 is formed to a thickness of roughly 100 Å to 500 Å, with 200 Å being optimal. This would be 0.01 μm to 0.05 μm, far below the thickness of the thermal silicon oxide layers described by applicant.

Applicant contends that one skilled in the art, prior to reading applicant's disclosure, would consider the thickness of a thermal oxide layer to be the distance measured from the

silicon/silicon oxide interface from which the silicon oxide is generated to the upper surface of the silicon oxide layer overlying that interface.

This question regarding the meaning of "thickness" is not one of impact, however, as the reference cited pertains to oxide thicknesses which are a factor of 10 less than the oxide thicknesses of interest to applicant. Applicant has indicated in his application Specification that his principal interest is silicon oxide layers having a thickness greater than 3 μm to handle particular applied voltages. (Paragraph 12) The Examiner has equated 3, 000 angstroms with 3 μm, however, angstroms are 10^{-10}, whereas micrometers are 10^{-6}, so 3,000 angstroms would be 0.3 μm and not 3 μm.

One method of amending applicant's claims to clearly distinguish the Witek et al. reference is to place the 3 μm minimal thickness requirement in applicant's independent claims. However, it appears it would be even more helpful to amend applicant's independent Claims 1, 12, 16,and 29 to more clearly indicate how the "thickness" of applicant's thermal oxide layer is produced. With this in mind, applicant's independent claims 1, 12, 16, and 29 have been amended to provide a three dimensional description of how the thermal oxide is formed in applicant's inventive method. In some instances a 3 μm minimal thickness recitation is provided, where appropriate.

For example, Claim 1 now recites that a silicon layer is etched to produce a plurality of adjacent trenches separated by a plurality of trench walls, where a thermally oxidized silicon oxide layer is produced which has a thickness approximately equal to the trench wall height and a width or a length which is greater than the sum of the plurality of trench opening widths. For this to occur without use of a fill oxide such as TEOS requires the conversion of the entire wall between trenches to silicon oxide. This does not occur in the Witek et al. reference and is not even suggested.

Claim 12 now recites that the thickness of the silicon oxide layer is equal to a height of an opening which is part of a plurality of openings used to create the oxide layer, and the height is at

least 3 μm. A silicon oxide thickness of at least 3 μm is not even suggested in the Witek et al. reference, which pertains to shallow trenches.

Claim 16 recites the formation of a shaped electrically isolated region in a silicon structure, where a first opening is etched a nominal distance into a first side of a silicon structure and a second opening is etched a n opening is etched a nominal distance into a second side of a silicon structure, where the first and second sides of the structure are directly opposed. The structure is then thermally oxidized to provide a thermally oxidized silicon oxide layer having a thickness approximately equal to the sum of the first nominal distance and the second nominal distance. The Witeck et al. reference neither teaches or even suggests the invention as presently claimed in Claim 16.

Claim 29 pertains to a method of creating isolation regions in a silicon structure where a plurality of openings are etched through a silicon structure to create a shaped portion separated by spokes between the plurality of openings, the structure is thermally oxidized to convert the spokes to silicon oxide. The Witeck et al. reference does not mention spokes, but even if a trench wall is considered to be a spoke, there is no instance where the entire thickness of a silicon wall between etched openings is converted to silicon oxide.

In more detail, according to applicant's invention, the percentage of a trench in a silicon layer which is filled with silicon oxide during the thermal oxidation process is a function of the thickness of the walls between the trenches and the width of the trench opening. For purposes of example, one micron of silicon would be converted to about 2 μm of silicon oxide during thermal oxidation. However, the oxidation reaction is diffusion limited, so when the walls become too thick, the conversion requires a time period which becomes impractical. Having selected an acceptable wall thickness, to completely fill the trench with silicon oxide, the trenches should be etched such that the width of the trench opening is about two times the thickness of the trench wall. (Page 4, line 20, through Page 5, line 3, and Page 10, lines 13 - 15, of applicant's Specification)

Applicant has indicated that a silicon oxide layer which is produced by their method should typically range between about 3 μm to about 200 μm to be practical. Support for this contention is found in applicant's Specification as originally filed in Paragraphs 12, 43, and 44, for example.

The Examiner cites Col. 6, line 54, through Col. 7, line 8, of Witek et al., which reads as follows: "FIG. 7 illustrates that the trench 210 and the polysilicon masking layer 206 are exposed to an oxidation ambient. This oxidizing ambient results in the formation of a thermal oxide liner 212 along vertical sidewalls in a bottom portion of the trenches 210 illustrated in FIG. 7. The same oxidation ambient will result in a polysilicon oxide (polyox) being formed along the sidewall and top portion of the polysilicon masking layer 206. This polysilicon oxidation will form a polysilicon oxide layer 214a as illustrated in FIG. 7. Generally, polysilicon will oxidize at a faster rate than single crystal silicon whereby the layer 214a and the layer 212 will be of different thicknesses, with layer 214a generally having a thicker dimension. It is preferred that the polysilicon masking layer 206 partially remains in FIG. 7 after the step of liner oxidation. Full consumption of the layer 206 by the sidewall liner oxidation process, while not being extremely problematic, may complicate the chemical mechanical polishing processes which are to following in subsequent figures. Generally, the liner 212 is formed to a thickness of roughly 100 Å to 500 Å with roughly 200 Å being optimal. At a 200 Å optimal thickness, the layer 214a will be roughly 200 Å to 300 Å thick."

The Witek et al. reference teaches the formation of a thin thermal oxide liner having a thickness of about 100 Å (0.01 μm) to about 500 Å (0.05 μm). Applicant's claimed invention pertains to the formation of thick thermal oxide layers having a thickness of about 3 μm (30,000 Å) to about 200 μm (2,000,000 Å).

Col. 7, lines 13 - 19, of Witek et al. reads as follows: "FIG. 8 illustrates that a trench fill material 216a is deposited, sputtered, or spin-coated over a top surface of the wafer 202. This layer 216a is preferably an ozone TEOS material, a furnace TEOS material, a high density

plasma (HDP) oxide, or some combination thereof. Generally, the trench fill layer is deposited to a thickness of roughly 3000 Å to 9000 Å." In other words, Witek et al. is using conventional deposition techniques (such as deposition from TEOS) to form a fill oxide layer. By contrast, applicant's claimed invention allows one to form thick silicon oxide layers using only a thermal oxidation process. As indicated in the teachings of both applicant and the Witek et al. reference, a thermal oxide has considerably different properties from oxides produced by other means. Further, applicant's invention requires only an oxygen ambient and a furnace, and does not require the use of other materials, such as TEOS.

Witek et al. does not teach or even suggest applicant's claimed invention. In light of the above distinctions and the amendments to independent Claims 1, 12, 16, and 29, applicant respectfully requests withdrawal of the rejection of Claims 1, 2, 5, 6, 10 - 17, 19, 20, 29, 30, and 32 under 35 USC § 102(b), over Witek et al.

Claims 12 - 17 and 20 are rejected under 35 USC § 102(e) as being anticipated by U.S. Patent No. 6,197,658, to Jang.

Applicant respectfully contends that the Jang et al. reference does not anticipate nor render obvious applicant's claimed invention.

The Jang reference pertains to distinguishable subject matter in general, as one skilled in the art can clearly see that Jang pertains to a method for filling a trench within a silicon substrate which does not convert any substantial portion of the walls surrounding the trench into silicon oxide. A silicon substrate is provided having a trench formed therein. A gap-filling silicon oxide trench fill layer is then formed upon the substrate and within the trench using an ozone assisted thermal chemical vapor deposition (SACVD) method. Densification of the gap-filling silicon oxide trench fill layer is carried out by annealing in an oxidizing atmosphere at an elevated temperature. The gap-filling silicon oxide trench fill layer is then planarized by CMP planarization. (Abstract)

Jang utilizes the technique of ozone assisted thermal chemical vapor deposition (SACVD) to form a silicon oxide trench fill layer. For example, at Col. 6, lines 47 - 52, Jang states as follows: "Within the first preferred embodiment of the method of the present invention, the gap filling silicon oxide trench fill layer 14 is preferably formed by ozone assisted sub-atmospheric pressure thermal chemical vapor deposition (SACVD) employing tetra-ethyl-ortho-silicate (TEOS) as a silicon source gas." Jang's silicon oxide trench fill layer is subsequently densified by annealing in an oxidizing atmosphere at an elevated temperature.

By contrast, applicant's amended independent Claims 12 and 16 pertain to a method of forming an electrically isolating region in a structure where it is conversion of a portion of the structure itself which provides the electrically isolating silicon oxide. Applicant's claimed invention allows one to form thick silicon oxide layers using only a thermal oxidation process. Applicant's silicon-containing trench walls serve as applicant's only silicon source, and applicant's invention does not require the use of an additional silicon source, such as TEOS.

With respect to Claim 12, the Jang reference does not teach or even suggest a method which provides for the formation of thermally oxidized silicon oxide layers having a thickness greater than about 3 μm. With respect to Claim 16, the Jang reference does not teach or even suggest etching the substrate from two opposing directions and then oxidizing the substrate to form a continuous layer of silicon oxide having a thickness approximately equal to the sum of the distances etched from the opposing directions.

In light of the above distinctions, applicants respectfully request withdrawal of the rejection of Claims 12 - 17 and 20 under 35 USC § 102(e), over Jang.

Claim Rejections Under 35 USC § 103

Claims 3, 4, 18, and 31 are rejected under 35 USC § 103(a) as being unpatentable over Witek et al., in view of Jang.

Claims 3 and 4 depend from independent Claim 1; Claim 18 depends from independent Claim 16; and Claim 31 depends from independent Claim 29. Claims 3, 4, 18, and 31 are patentable over the combination of Witek et al. and Jang for the same reasons that Claims 1, 16, and 29 are patentable over Witek et al.

The deficiencies of the disclosures of Witek et al. and Jang with respect to the patentability of the present invention are discussed in detail above with respect to the rejections of various claims under 35 USC § 102. A combination of these references does not even suggest applicant's invention as claimed in applicant's amended claims, for the reasons provided above.

In light of the above distinctions and the amendments to independent Claims 1, 16, and 29, applicant respectfully requests withdrawal of the rejection of Claims 3, 4, 18, and 31 under 35 USC § 103(a), over Witek et al., in view of Jang.

Claim 7 is rejected under 35 USC § 103(a) as being unpatentable over Witek et al., in view of U.S. Patent No. 6,355,540, to Wu.

The deficiencies of the disclosure of Witek et al. with respect to the patentability of the present invention are discussed in detail above with respect to the rejection of Claims 1, 2, 5, 6, 10 - 17, 19, 20, 29, 30, and 32 under 35 USC § 102(b).

Wu pertains to a method for forming a shallow trench isolation region in a semiconductor substrate for ULSI devices. The trench region includes a thermal oxide film formed on the bottom and the sidewall, a CVD dielectric film formed on the bottom of the thermal oxide film, and a channel stop region formed beneath the bottom of the thermal oxide film. Forming a pad oxide / silicon nitride layer on the substrate, the trench region and active area are defined. After silicon spacers are formed, the silicon substrate is recessed to form a trench region by using the silicon nitride layer and silicon spacers as an etching mask. Then, a thermal oxide film is regrown on the trench surface. After removing the silicon nitride layer, a thick CVD dielectric

layer is deposited on the substrate. The dielectric film outside the trench region is removed by a CMP process. (Abstract)

At Col. 4, lines 29 - 52, Wu describes forming a thermal oxide layer 14 on the trench surface, followed by deposition of a thick dielectric layer 16 over the semiconductor substrate 2, to fill the trench (shown in Fig. 8). As set forth a Col. 4, lines 44 - 52: "The suitable method for forming this thick dielectric layer 16 can be LPCVD, PECVD (plasma-enhanced CVD) or HDPCVD (high-density plasma CVD) with the material of silicon nitride, silicon oxynitride, or silicon oxide, including tetra-ethyl-ortho-silicate-oxide (TEOS-oxide), ozone TEOS-oxide, boro-phospho silicate glass (BPSG), phospho silicate glass (PSG), borosilicate glass, (BSG), undoped silicate glass (USG) or silicon-rich oxide (SRO), and so on."

Like Jang, Wu utilizes chemical vapor deposition techniques to form a thick dielectric layer. As discussed above, applicant's claimed invention does not require the use of chemical vapor deposition processes. Applicant's claimed invention allows one to form thick silicon oxide layers using only a thermal oxidation process. Applicant's silicon-containing trench walls serve as applicant's only silicon source, and applicant's invention does not require the use of an additional silicon source, such as TEOS.

The Examiner cites Wu as teaching anisotropic reactive ion etching using a fluorine-containing etchant component. The nonobviousness of applicant's Claim 7 is not based on the use of a fluorine-containing etchant to etch a silicon-containing substrate, but is based on the combination of elements recited in the dependent claim in combination with claims from which it depends. Claim 7 depends from Claim 1. Applicant maintains that Claim 7 is patentable over the combination of Witek et al. and Wu for the same reasons that Claim 1 is patentable over Witek et al.

Whether taken alone or in combination, neither Witek et al. nor Wu teaches or even suggests applicant's claimed invention. In light of the above distinctions and the amendment to

independent Claim 1, applicant respectfully requests withdrawal of the rejection of Claim 7 under 35 USC

§ 103(a) over Witek et al., in view of Wu.

Claims 8 and 9 are rejected under 35 USC § 103(a) as being unpatentable over Witek et al., in view of U.S. Patent No. 6,482,718, to Shiozawa et al.

Claims 8 and 9 depend from Claim 1, and pertain the aspect ratio of the trench height to the trench opening width. This is important in terms of the amount of time required to oxidize the silicon to produce a silicon oxide layer having a thickness of approximately the trench height.

The deficiencies of the disclosure of Witek et al. with respect to the patentability of the present invention are discussed in detail above with respect to the rejection of Claims 1, 2, 5, 6, 10 - 17, 19, 20, 29, 30, and 32 under 35 USC § 102(b).

Shiozawa et al. pertains to a method of manufacturing a semiconductor device which is said to prevent degradation in the operating characteristics of semiconductor elements which are isolated from each other by an element isolation region in a trench isolation structure. Implantation of ions in a polycrystalline silicon layer from above through a silicon nitride film produces an ion-implanted polycrystalline silicon layer. The implantation of the ions changes the polycrystalline silicon layer into an ion-implanted polycrystalline silicon layer which is said to have a higher oxidation rate. In subsequent formation of a thermal oxide film on the inner wall of a trench, an exposed part of the ion-implanted polycrystalline silicon layer is also oxidized, forming relatively wide polycrystalline silicon oxide areas. (Abstract)

Shiozawa utilizes the technique of ion implantation to increase the oxidation rate of a polysilicon film. At Col. 6, lines 22 - 51, Shiozawa et al. states: "Then, as shown in FIG. 5, thermal oxidation is performed to form a thermal oxide film 21 on the inner wall of the trench 5. The thermal oxide film 21 is formed in such a manner that silicon on the inner-wall surface of the trench 5 is oxidized to an oxide film. Since about half of the thermal oxide film 21 in thickness

is formed inwardly from the interface of the trench 5 of FIG. 4, a resultant opening 22 has a smaller width than the opening 20. The thickness of the thermal oxide film 21 is determined to be not more than 50 nm [0.05 μm] so that the width (opening) 22 of the trench 5 after the formation of the thermal oxide film 21 is not less than the critical width of a filling material used in a subsequent process step. At this time, the ion-implanted polycrystalline silicon layer 16 and exposed part of the silicon nitride film 2 are also oxidized, forming polycrystalline silicon oxide areas 21a (the oxidation of the silicon nitride film 2 is not shown). Since the oxidation of the ion-implanted polycrystalline silicon layer 16 is accelerated by the ions 15 and thus the oxidation rate of the ion-implanted polycrystalline silicon layer 16 is higher than those of the polycrystalline layer 3 and the silicon substrate 1, the ion-implanted polycrystalline silicon layer 16 is oxidized over a wider range than the thickness of the thermal oxide film 21. For example if the oxidation rate of the ion-implanted polycrystalline silicon layer 16 is twice that of the polycrystalline silicon layer 3 by the oxidation accelerating effect of the ions 15, the polycrystalline silicon oxide areas 21a also become twice as wide as what they are formed in the polycrystalline silicon layer 3." In other words, the maximum thickness of the silicon oxide film which is formed by thermal oxidation according to the method of Shiozawa et al. is approximately 100 nm (0.1 μm).

At Col. 6, lines 58 - 64, Shiozawa et al. states as follows: "Then, as shown in FIG. 6, a buried oxide film (buried layer) 8 is formed to fill the trench 5 and to cover the whole surface, by TEOS, HDP, CVD, or the like."

Like the Jang and Wu references, the Shiozawa et al. reference utilizes chemical vapor deposition techniques to form a thick dielectric layer. As discussed above, applicant's claimed invention does not require the use of chemical vapor deposition processes. Applicant's claimed invention allows one to form thick silicon oxide layers using only a thermal oxidation process. Applicant's silicon-containing trench walls serve as applicant's only silicon source, and applicant's invention does not require the use of an additional silicon source, such as TEOS.

The Examiner cites Shiozawa et al. as teaching specific trench aspect ratios. Applicant is not relying on the trench aspect ratio as the sole element of nonobviousness for Claims 8 and 9. At page 10, lines 12 - 13, of applicant's specification, applicant states that "Known plasma etching techniques enable the etching deep trenches having an aspect ratio as high as 50 : 1." It is a combination of the elements in the claims from which these claims depend with the aspect ratios recited in these claims which is nonobvious. It is this combination which enables not only the formation of thick thermal oxide layers, but the production of such thick layers in an economically reasonable time, as discussed in applicant's Specification.

Neither Witek et al. nor Shiozawa et al. teaches or even suggests a method which provides for the formation of thermally oxidized thick silicon oxide layers formed in the manner claimed by applicant. Even if one were to combine the disclosure of Shiozawa et al. with that of Witek et al., one would not arrive at applicant's claimed invention.

In light of the above distinctions and the amendment to independent Claim 1, applicant respectfully requests withdrawal of the rejection of Claims 8 and 9 under 35 USC § 103(a) over Witek et al., in view of Shiozawa et al.

Claims 21, 22, and 24 are rejected under 35 USC § 103(a) as being unpatentable over Jang, in view of U.S. Patent No. 6,084,257, to Petersen et al.

As discussed above, the Jang reference teaches the technique of ozone assisted thermal chemical vapor deposition (SACVD) to form a silicon oxide thick trench fill layers. Jang does not teach or even suggest the use of thermal oxidation to form thick silicon oxide layers.

Petersen et al. pertains to a single-crystal silicon sensor with a high aspect ratio and curvilinear structures. A semiconductor sensor includes a first single-crystal silicon wafer layer having a single-crystal silicon structure formed therein. The structure includes two oppositely disposed substantially vertical major surfaces, and two oppositely disposed generally horizontal minor surfaces. The aspect ratio of a major surface to a minor surface is at least 5 : 1. A carrier

which includes a recessed region is secured to the first wafer layer such that the structure is suspended opposite the recessed region. (Abstract)

The Petersen et al. reference is cited by the Examiner a teaching a step of fusion bonding a plurality of silicon structures to provide at least one continuously oxidized region through the bonded structure. In particular, the Examiner refers to Col. 7, lines 15 - 45 of the Petersen et al. reference.

At Col. 7, lines 31 - 37, Petersen et al. states as follows: "The silicon fusion bonding technique described above bonds the first and second wafers together without the use of an intermediate glue material that could have a different coefficient of thermal expansion than the single crystal silicon wafers. Furthermore, fusion bonding can be performed in which oxide or nitride layers have been formed in the bonded surfaces of one or both wafers."

Applicant's independent Claim 21 (from which Claims 22 and 24 depend) has been amended to reflect more closely the series of method steps described in Figure sets 2 and 3 and the accompanying description in applicant's Specification. Although Petersen suggests that wafers to be bonded could include oxide or nitride layers, Petersen et al. does not disclose forming, by thermal oxidation, a silicon oxide region which passes entirely through a multi-layered bonded structure, with subsequent creation of an electrically isolated through hole in the silicon oxide region. Even if one were to combine the disclosure of Petersen et al. with that of Jang, one would not arrive at applicant's claimed invention.

Whether taken alone or in combination, neither Jang nor Petersen et al. teaches or even suggests applicant's invention as claimed in Claims 21, 22, and 24. In light of the amendments to Claim 21, and the above distinctions, applicant respectfully requests withdrawal of the rejection of Claims 21, 22, and 24 under 35 USC § 103(a) over Jang, in view of Petersen et al.

Claim 23 is rejected under 35 USC § 103(a) as being unpatentable over Jang, in view of Petersen et al., and further in view of U.S. Patent No. 6,338,284, to Najafi et al.

The deficiencies of the disclosures of Jang and Petersen et al. with respect to the patentability of the present invention are discussed in detail above with respect to the rejection of Claims 21, 22, and 24.

Najafi et al. pertains to structures and methods for fabrication of electrical lead transfer feedthroughs with respect to a sealed cavity. In some applications such as capacitive pressure sensing, the cavity may include an outer wall, in which case the electrically insulating barrier is preferably U-shaped, with the ends of the U terminating at the outer wall. The feedthrough section may alternatively take the form of an island of conductive material surrounded by the electrically insulating barrier, thus assuming an O shape. The cavity may be evacuated or filled with specific gases at specific pressures. (Abstract)

Claim 23 depends from Claim 21. Claim 23 recites that the bonding of one silicon structure layer to another is performed using eutectic bonding. Najafi et al. is cited by the Examiner as disclosing the use of diffusion bonding or eutectic bonding to attach different substrates to each other. However, applicant is not relying on the eutectic bonding technique alone to render Claim 23 nonobvious. It is the combination of the recitations in Claim 23 and Claim 21 from which it depends which is nonobvious. Applicant maintains that Claim 23 is patentable over the combination of Jang, Petersen et al., and Najafi et al. for the same reasons that Claim 21 is patentable over Jang and Petersen et al.

Whether taken alone or in combination, neither Jang, nor Petersen et al., nor Najafi et al. teaches or even suggests applicant's claimed invention. In light of the above distinctions, applicant respectfully requests withdrawal of the rejection of Claim 23 under 35 USC § 103(a), over Jang, in view of Petersen et al., and further in view of Najafi et al.

Claims 25 - 28 are objected to as being dependent upon a rejected base claim, but are said to be allowable if rewritten in independent form to include all of the limitations of the base claim

and any intervening claims. Since the recitation of Claim 26 was added to amended Claim 21, applicant contends that Claims 21 - 25 and 27 - 28 are now allowable.

Applicant respectfully contends that the presently pending claims as amended are in condition for allowance, and the Examiner is respectfully requested to enter the present amendments and to pass the application to allowance.

The Examiner is invited to contact applicant's attorney with any questions or suggestions, at the telephone number provided below.

Respectfully submitted.

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